DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE

Mid Semester Examination – Oct 2018

Course: B. Tech in S.Y. (ECT) **Sem: III**

Subject Name: Network Analysis **Subject Code: BTEXC304**

Max Marks: 20M **Date:-11/10/2018** **Duration:- 1 Hr.**

Instructions to the Students:

1. Check Question paper correct or not.
2. Draw net and labeled circuit diagram.
3. Use appropriate units with entities.
4. Assume suitable data if required.

Marks

Q. 1 Attempt following questions **6**

1 An attenuator is a
(A)R's network. (B)RL network.
(C)RC network. (D)LC network.

2 How is the loop analysis different in application/functioning level as compared to Kirchoff's law?
(A) Utilization of loop currents instead of branch currents for writing equations
(B) Capability of branch current to carry multiple networks
(C) Reduction in the number of unknowns for complex networks
(D)All of the above

3 What would be the value of power factor for series RLC circuit under the resonance phenomenon?

(A) 0 (B)0.5 (C) 1 (D) Infinity

4 Kirchhoff s current law states that

(A) net current flow at the junction is positive

(B) Algebraic sum of the currents meeting at the junction is zero

(C) no current can leave the junction without some current entering it.

(D) total sum of currents meeting at the junction is zero

5 A Star connection contains three impedances of 60 Ω each. The impedances of equivalent delta connection will be
(A)120Ω each. (B)160Ω each. (C)180 Ω each. (D)60Ω each.

6 Thevenin resistance Rth is found

(A) by removing voltage sources along with their internal resistances

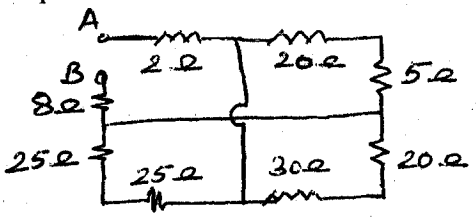
(B) by short-circuiting the given two terminals

(C) between any two 'open' terminals

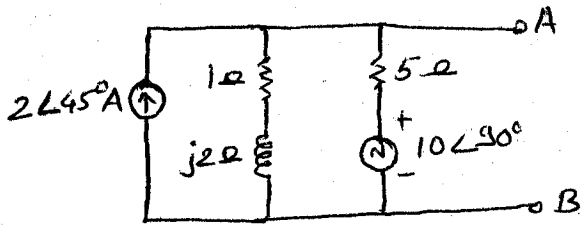
(D) between same open terminals as for Eth

Q.2 Solve Any Two of the following. **3 X 2**

(A) Find the equivalent resistance between A&B in the network of Figure.



(B) Find Thevenin's equivalent network across terminals A&B for figure



(C) Derive the equation of resonant frequency for RLC series Resonance with circuit diagram & phasor representation of Voltage & Current.

Q. 3 Solve Any One of the following. **8**

(A) Each of the two series elements of a T-section low pass filter consists of an inductor of 60mH having negligible resistance and a shunt element having a capacitance of 0.2μf. Calculate a) the cut-off frequency b) nominal impedance c) Characteristic impedance at frequencies of 1KHz & 5KHz.

(B) A resistor and a capacitor are connected in series with a variable inductor .When the circuit is connected to a 230V,50Hz supply, the maximum current obtained by varying the inductance is 2A .The voltage across the capacitor is 500V. Calculate resistance, Inductance & capacitance of the circuit.

***** End *****

DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE – RAIGAD -402 103
Mid Semester Examination – October - 2018

Branch: (SY)B.Tech (ECT-Analog Circuit) **Sem.:- III**

Subject with Subject Code:- BTEXC302 **Marks: 20**
Date:- 09/10/2018 **Time:- 1 Hr.**

Instructions:- **(Marks)**

1. Check weather you have got correct question paper.
2. Assume suitable data if necessary.
3. Figure to right indicates full marks.

Q.No.1 **Attempt Following questions** **(06)**

1) Higher the value of Re-------is –Ve feedback -------is common mode gain ?
   a.) More,Less b.) Less,Less c.) More More.
2) Op-Amp 741 IC uses a -------polarity supply?
   a.) Dual b.) Single c.) Negative.
3) Input resistance of inverting amplifier is -------?
   a.) Zero b.) One c.) ∞.
4) Inverting amplifier introduces -------feedback?
   a.) Positive b.) Negative C.) Non of these
5) --------is also known as regenerative comparator.
   a.) Schmitt trigger b.) Inverting c.) non inverting comparator.
6) The Schmitt trigger used -------- feedback.
   a.) Positive b.) Negative c.) No feedback.

Q.No. 2 **Attempt any Two of the following:** **(06)**

a.) Discuss following parameters of an Op-Amp:
   1.) Slew rate 2.) Input Offset voltage 3.) SVRR.
b.) Define Integrator? And prove the expression for output voltage ?
c.) Design a Schmitt trigger whose VLT and VUT are ± 5V, Draw it's wave form.
Note:- Vsat= ± 12V, Supply voltage =± 15V.

Q.No.3 **Solve any one** **(08)**

a.)What is need of level shifter in op-amp? Draw the block diagram of op-amp and explain each block in detail?
b.) What is need of instrumentation amplifier? sketch instrumentation amplifier using three op-amp' and derive it's output expression?

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DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE

Mid Semester Examination – Oct 2018

Course: B. Tech in Electronics & Telecommunication Engineering **Sem: III**

Subject Name: Digital Logic Design **Subject Code: BTEXC305**

Max Marks: 20 **Date:- 12-10-18** **Duration:- 1 Hr.**

Instructions to the Students:

1. **Figure to right indicate full marks**
2. **Assume suitable data whenever necessary**

Marks

Q. 1 **6**

1. The NOR logic gate is the same as the operation of the _____ gate with an inverter connected to the output.

A. AND
B. OR
C. NAND
D. None of Above

2. When grouping cells within a K-map, the cells must be combined in groups of _____.

A. 2's
B. 3's
C. 1,2,4,8…Etc.
D. 4's

3. How is a *J-K* flip-flop made to toggle?

A. J = 0, K = 0
B. J = 0, K = 1
C. J = 1, K = 0
D. J = 1, K = 1

4. Which of the following is correct for a Clocked *D* flip-flop?

A. The output toggles if one of the inputs is held HIGH.
B. Only one of the inputs can be HIGH at a time.
C. The output complement follows the input when enabled.
D. The output complement follows the input when enabled.

5. Which type of memory elements are used in synchronous sequential circuits?

a. Clocked Flip flops
b. Unclocked Flip flops
c. Time Delay Elements
d. All of the above

6. The major difference between a moore and mealy machine is that

A. output of the former depends on the present state and present input
B. output of the former depends only on the present state
C. output of former depends only on the present input
D. None of Above.

Q.2 Solve Any Two of the following. 3 X 2

(A) Solve K- Map for the equation

$F = \pi M (1,2,3,4,,6,7,8 ,) + d(4,5)$

(B) Convert JKFF to TFF

(C) Draw and explain four bit Universal Shift Register.

Q. 3 Solve Any One of the following. 8

(A) Design sequence generator using Mealy Machine for sequence 1 1 0

(B) Design 3- bit UP Counter.

*** End ***

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DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE

Mid Semester Examination – Oct 2018

Course: B. Tech in Electronics and Telecommunications Engg. **Sem: III**

Subject Name: Electronic Devices and Circuits **Subject Code: BTEXC303**

Max Marks: 20 **Date:- 10/10/2018** **Duration:- 1 Hr.**

Instructions to the Students:

1. Verify that you got correct question paper.
2. Figures to right indicate full marks.
3. Assume suitable data wherever necessary.

Marks

Q. 1 Solve the following **6**

1. _____ is not a Region of operation for JFET?

   a) Cut-off b) Ohmic c) Saturation d) Linear

2. The voltage at which JFET goes into cut off is called as pinch off voltage.

   a) True b) False

3. The minimum gate source voltage that creates an inversion layer is called

   a) cut off voltage b) on voltage c) threshold voltage d) zener voltage

4. Common base is one of the configurations of MOSFET amplifier.

   a) True b) False

5. The bandwidth using negative feedback

   a) Increase b) Decreases c) Remains constant d) None of these

6. The overall gain can be increased using multi stage amplifier

   a) True b) False

Q.2 Solve Any Two of the following. **3 X 2**

a) Calculate the transconductance of a JFET when reverse gate to source voltage changes from 4V to 3.9V causes change in drain current from 1.3 mA to 1.6 mA.

b) List the biasing methods of MOSFET. Draw a neat circuit diagram of any two.

c) Compare and contrast: Voltage series feedback, Voltage shunt feedback, Current series feedback, Current shunt feedback.

Q. 3 Solve Any One of the following. **8**

a) Draw and explain the construction and working of n channel EMOSFET.

b) Analyze the effect of negative feedback on terminal characteristics of an amplifier.

***** End *****

SE 28 40

DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE

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