

MGM UNIVERSITY

J.N.E.C. AURANGABAD

DEPARTMENT OF ELECTRONICS & TELECOMMUNICATION

F.Y.-M.TECH. (VLSI & ES)

Year: 2021-22 (Semester -II)

**Course Code: 20PET204EB: Elective 3: ARM CONTROLLERS.**

End SEM Exam

Max Marks: 60

Time: Three Hours

N.B. (I) All six questions are compulsory.

(II) Assume suitable additional data if necessary.

Q1. What is an embedded system? List and define the main characteristics of embedded systems. [10]

Q2. Describe the salient features of ATMEL AVR microcontroller. [10]

Q3. Write a PIC based assembly language program to toggle the SFR of PORT B and PORT C

Continuously. [10]

OR

What is interrupts vs. polling method of data transfer? What are the steps in executing an

Interrupt? Discuss interrupt vector table for the PIC18. [10]

Q4. Describe the important features that make ARM ideal for embedded applications. [10]

Q5. Write ARM based assembly language program to evaluate the expression

$3X+9Y+9Z$  Where  $X=2$ ,  $Y=3$ ,  $Z=4$  [10]

OR

Discuss thumb instruction set available in ARM processor. [10]

Q6. Describe and discuss Data Processing Instructions in ARM. [10]

Name of the Program :F.Y.-M.TECH. (VLSI & ES)

Semester :2021-22 (Semester -II)

Course Code: 20PET203B

Name of the Course:Internet of Things

Max Marks: 60

Time: Three hours

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Instructions:

(I)All questions are compulsory.

(II)Each question carries equal marks.

(III)Assume suitable additional data if necessary.

Q. 1. What is the function of Device Power of IoT (10)

Q.2) Explain an ITU-T views, in Internet of things... (10)

OR

Q.2) Define of the Scalability of IOT

Q.3) Explain the RFID middleware architecture (10)

Q.4) What is a wireless sensor network? Explain node in WSN. (10)

OR

Q.4) Comparison of WPAN technologies cellular & mobile network technologies for IoT/M2M

Q.5) Explain the Aspects of governance Bodies subject to governing principles (10)

Q.6) Explain block diagram of Smart Metering using Arduino. (10)

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**Mahatma Gandhi Mission University**  
**Second Sem Exam (AY2021-22)-JUNE2022**

**College: Jawaharlal Nehru Engineering College**

**Course Code: 20PET201D**

**Name of the Course: Digital CMOS VLSI Design**

**Class: MTech. (VLSI and Embedded system)**

**Marks : 60**

**Time: 3:00Hr.**

**Instructions to the Students**

- 1) All Questions compulsory
- 2) Neat Diagrams must be drawn wherever necessary.
- 3) Figures to the right indicate full marks.
- 4) Use of calculator is allowed.

Q1] a) With the help of  $I_{ds}$  equations describe behavior of NMOS device in cut-off, linear and saturation region. Draw all stages. [10]

**OR**

b) Draw C-V Characteristics of MOSFET and describe in detail. [10]

Q2] a) Design following function using compound gate CMOS and verify with Example

i)  $F = AB + DE + C$

ii)  $F = AB + C(D + E)$

[10]

**OR**

b) What is mean by transmission gate? Draw symbol and write advantage of transmission gate. Design 2:1 MUX using transmission Gate [10]

Q3] a) Describe layout design Rules. Enlist layout tools and explain Microwind tool in detail. [10]

**OR**

b) Design Two input NAND Gate using CMOS. Draw DC voltage transfer characteristics for two input NAND Gate and explain in detail. [10]

Q4] a) Describe Pseudo-NMOS Logic . Draw diagram for DCVSL(Differential cascode voltage switch logic) and explain in detail. [10]

**OR**

b) Describe Dynamic combinational logic with diagram and waveform. Also Design Dynamic Circuit :  $A.B + C$  and explain it. [10]

Q5] a) Draw Two input CMOS NAND Gate and Calculate Logical Effort , Parasitic delay of CMOS Two Input NAND Gate. [10]

**OR**

b) What is difference between Flip Flop and Latches? Explain One phase Systems for Flip-Flops and Two phase systems for Latches. [10]

Q6] a) Describe flowing non ideal effects i) Velocity saturation and Mobility degradation  
ii) Hot carrier effect    iii) Body effect and early effect in MOSFET [10]

**OR**

b) Find a equivalent CMOS inverter circuit for simultaneous switching of all inputs assume that  $(W/L)_p = 15$  for all PMOS transistor and  $(W/L)_n = 10$  for all NMOS transistor for the following Boolean Equations:  $F = (C + D + E).(A + B)$ . [10]



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- 3) Figures to the right indicate full marks.
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b) Find a equivalent CMOS inverter circuit for simultaneous switching of all inputs assume that  $(W/L)_p = 15$  for all PMOS transistor and  $(W/L)_n = 10$  for all NMOS transistor for the following Boolean Equations:  $F = (C + D + E).(A + B)$ . [10]



**MGM University**  
**Aurangabad-431003**  
**Second Term Exam A.Y. 2021-22**

Program : M.Tech (VLSI and Embedded Systems)

Course : Analog CMOS VLSI Design

Course Code : 20PET202D

Sem –II  
Marks : 60

Instructions to the students

1. Each question carries 10 marks.
2. All questions are compulsory.
3. Assume suitable data wherever necessary.

Marks

Q1. Solve any two

- a) Sketch the structure of NMOS transistor and explain cut-off, linear and saturation regions of operation. (5)
- b) Draw and explain the three input NAND standard cell gate layout. (5)
- c) Write a short note on MOS resistor. (5)

Q2. Solve any two

- a) What is sub-threshold MOS model? Explain with neat suitable diagram. (5)
- b) Write a short note on CMOS device modelling. (5)
- c) Explain various computer simulation models of MOS transistor. (5)

Q3. Solve any two

- a) Draw and explain wilson current mirror model using CMOS. (5)
- b) Apply the principle of bandgap voltage reference to design a Reference Voltage Source. Derive the coefficient of the thermal voltage ( $kT/q$ ) for bandgap voltage reference. (5)
- c) Explain the operation of a MOS device as a switch. (5)

Q4. Solve any two

- a) Find the small-signal current gain,  $A_i$ , the input resistance,  $R_{in}$ , the output resistance,  $R_{out}$ , and the -3dB frequency in Hertz for the current amplifier, if  $I_1 = I_2 = 100\mu A$  and  $W_2/L_2 = 10W_1/L_1$ . Assume that  $C_{bd1} = 10fF$ ,  $C_{gs1} = C_{gs2} = 100fF$ , and  $C_{gs2} = 50fF$ . (5)
- b) Explain high gain amplifier using CMOS. (5)
- c) Draw and explain voltage transfer characteristics of differential amplifier with current mirror load. (5)

Q5. Solve any two

- a) Define PSRR. Derive its expression for two stage Op Amp. (5)
- b) What is operational amplifier? Explain its block diagram. (5)
- c) Explain the design steps of Op Amp using CMOS. (5)

Q6. Solve any two

- a) Explain the operation of comparator in detail. (5)
- b) Enlist the applications of comparator. Explain any one in detail. (5)
- c) Write a short note on discrete time comparators. (5)





**MGM University**  
**Aurangabad-431003**  
**Second Term Exam A.Y. 2021-22**

Program : MTech (VLSI&ES)

Sem -II

Course : Network Security and Cryptography

Marks : 60

Course Code : 20PET205EB

Instructions to the students

1. Each question carries 10 marks.
- 2 All questions are compulsory
3. Illustrate your answers with neat sketches , diagram etc wherever necessary
4. If some part or parameter is noticed to be missing ,you may appropriately assume it and should mention it clearly

	Marks
Q1. Solve any two	
a) Draw and Explain OSI security architecture	(5)
b) Explain any one classical encryption technique.	(5)
c) Explain the need of network security	(5)
Q2. Solve any two	
a) Define Fermat's theorem	(5)
b) Give Euclidean algorithm	(5)
c) Explain modular arithmetic.	(5)
Q3. Solve any two	
a) State the data encryption standards.	(5)
b) Give the difference between linear and differential cryptanalysis.	(5)
c) Explain the block cyphers	(5)
Q4. Solve any two	
a) Explain elliptical curve cryptography,	(5)
b) What is message authentication code? Explain	(5)

c) Write a note on HMAC

(5)

Q5. Solve any two

a) Give the digital signature standards

(5)

b) Draw and explain the IP security architecture

(5)

c) Discuss web security considerations

(5)

Q6. Solve any two

a) What is intrusion ?What are its types?Explain

(5)

b) State the firewall design principles.

(5)

c) Explain the different countermeasures to be taken to protect the system

(5)

End of paper