Total No. of Printed Pages:2

SUBJECT CODE NO:- K-04
FACULTY OF ENGINEERING AND TECHNOLOGY
T.E. (EC/ECT/IE/E&C) Examination Oct/Nov 2016
Power Electronics
(Revised)

[Time:Three Hours] **[Max.Marks:80]**

Please check whether you have got the right question paper.

N.B i) Q.No.1 from section A and Q.No.6 from section B are compulsory.
ii) Attempt any two questions from Q.2 to Q.5 & also from Q.7 to Q.10 from each section.
iii)Assume suitable data if necessary.

Section A

Q.1 Solve any two 10

i) What would happen if positive gate voltage is given to reverse blocking thyristor? Justify.
ii) Diode reverse recovery characteristics.
iii) Step down cycloconverter.
iv) Dual converter

Q.2 a) "As Gate Current increases Break over voltage decreases". of an SCR", Justify. 07
b) For an SCR, the gate-cathode characteristic has a source voltage of 15V, a straight line scope of 130 & allowable gate power dissipation of 0.5 watts, compute the gate-source resistance. 08

Q.3 a) With the help of structure & V-I characteristics of DIAC, explain various operating modes of TRIAC. 07
b) The trr=5μbcc. & di/dt=80A/μs. If s.f.=0.5,determine 08
a) Q_{RR} b) I_{RR}

Q.4 a) Draw & explain the circuit diagram of 3-φ full converter with R-load with neat voltage & current waveforms? 07
b) A 1-φ 230V, 1KW heater is connected across 1-φ,230V, 50Hz supply through an SCR. For firing angle delays of 45^0 & 90^0, calculate the power absorbed in the heater element. 08

Q.5 a) Explain effect & source inductance on 1-φ full converter. 07
b) Explain on-off control method of A.C. voltage controller. 08

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Section B

Q.6 Solve any two, 10

i) Series inverter
ii) Class 'c' chopper
iii) HF heating
iv) 1-φ full bridge inverter

Q.7 a) With neat circuit diagram & wave forms. Explain working of 3- φ 120^0 conduction mode bridge inverter. 07

b) A 1-φ full bridge inverter is operated from 48v battery and a resistive load of 10Ω. Determine 08
1)O/P voltage of fundamental frequency
2)O/P RMS power
3) Thyristor rating

Q.8 a) Explain current commutated chopper with neat circuit diagrams & waveforms. 07

b) The dc chopper has a resistive load of R=10Ω, 1/p dc voltage is 220v. When the chopper switch remains on. Its ON-stage voltage drop is 2V. Chopper frequency is 1KHz. If duty cycle is 50%. Determine. 08
1) Average O/P Load Voltage
2) RMS O/P Load Voltage
3) Effective I/P Resistance

Q.9 a) Explain Time delay circuit with neat waveforms & circuit diagram. 07

b) Explain temperature controller with neat circuit diagram & waveforms. 08

Q.10 a) With the help of neat circuit diagram, derive the expression for minimum & maximum load current of class –A Chopper. 07

b) Explain various voltage control techniques of an Inverter. 08

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Total No. of Printed Pages:2

SUBJECT CODE NO:- K-25
FACULTY OF ENGINEERING AND TECHNOLOGY
T.E.(EC/ECT/E&C) Examination Oct/Nov 2016
Signal Coding & Estimation Theory
(Revised)

[Time:Three Hours] **[Max.Marks:80]**

Please check whether you have got the right question paper.

N.B i) Q.No.1.and Q. No. 5 are compulsory.
ii) Solve any two questions from each section from Q.no 2 to 4 and Q. No. 6 to 8.

Section A

Q.1 Solve any two 10
a) Mutual information.
b) Cascaded channel
c) LZW algorithm

Q.2 a) Derive an expression for entropy function. 07
b) The output of an information source consists of 150 symbols, 32 of which occur with a probability of $\frac{1}{64}$ and the remaining 118 occur with a probability of $\frac{1}{236}$. The source emits 2000 symbols / sec find the average information rate of this source. 08

Q.3 a) Explain source coding theorem. 07
b) Apply shannon fano algorithm for following message and find coding efficiency. 08

Message	M_o	M_1	M_2	M_3	M_4
Probability	0.55	0.15	0.15	0.10	0.05

Q.4 a) Find the channel capacity for binary erasure channel 07
b) A message source produces two independent symbols A and B with probabilities P(A) =0.4 and P (B) =0.6 if the symbols are received is average coitus4 in every 100 symbols is error, calculate the transmission rate of the system. 08

Section-B

Q.5 Solve any two 10
a) Perfect codes
b) Hamming codes
c) Goley codes

Q.6 a) Matrix description of linear block codes. 07
b) For a systematic (7,4) linear block code, the parity matrix is given by 08

$$[P] = \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 0 \\ 1 & 0 & 1 \\ 0 & 1 & 1 \end{bmatrix}$$

1) Find out code vectors
2) Parity check matrix
3) Draw encoder diagram for the above codes.

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Q.7 a) Explain circuit implementation of cyclic codes. 07

b) A (15,5) Cyclic code has $9(x)=1+x+x^2+x^4+x^5+x^8+x^{10}$ 08

1) Draw encoder diagram
2) Draw syndrome CKT
3) Find code polynomial $D(x) = 1+ x^2+x^4$

Q.8 a) Explain time domain and transfer domain approach of convolutional codes. 07

b) With an example explain in detail Viterbi algorithm. 08

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No. of Printed Pages:2

SUBJECT CODE NO:- K-55

FACULTY OF ENGINEERING AND TECHNOLOGY

T.E.(EC/ECT/IEC/E&C) Examination Oct/Nov 2016

Microcontroller & Advanced Processors

(Revised)

[Time:Three Hours] **[Max. Marks:80]**

Please check whether you have got the right question paper.

N.B i) Q.No.1 & 6 are compulsory.
ii)Answer three question from each section .
iii) Assume suitable data wherever necessary

Section- A

Q.1 Solve any two 10

a) Find physical address of

1. I) 4768:2246H ii) 9620:1A42H
2. If EV calculates EA if 2624& Ds register is 8000h, what is the physical address

b) Explain the following 8086 instructions

1. LES 2) IMUL 3) ADD 4) NEG 5) ROL

c) Explain BIU of 8086

Q.2 a) Explain string instruction with suitable examples 08

b) Explain the following

1) DUP 2) DW 3) PUBLIC 4) PROC 07

Q.3 a) With suitable example explain the various addressing modes of 8086 08

b) Write an 8086 based ALP to evaluate following expression 07

$Z=(A+B) \times (C=D)$

Q.4 a) Explain the interrupts of 8086. How does 8086 respond to the interrupted 08

b) Explain 8255 interfacing with 8086 07

Q.5 a) Design 8086 based system with following specification 08

1. 8086 in min mode 2) 8 KB RAM 3) 8KB EPROM

b) WAP using 8086 to transfer block of 10- bytes using string instructions 07

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Section –B

Q.6 Solve any two 10

a) Explain in detail features of 80286
b) Compare Microprocessor with Microcontrollers
c) WAP to generate a delay of 0.5µs with a crystal of 12MHr using timer in 8051

Q.7 a) Explain the detail architecture of 80286 08

b) Explain

1) $\overline{PSEN}$ 2) RST 3) ALE 4) $\overline{INTR}$ 07

Q.8 a) Design a 8051 based system with the following specifications 08

1) 8 KB of EPROM
2) 4 KB of RAM

Give the memory map of the system 07

b) Explain the following instructions of 8051

1. SWAP A
2. MOVX
3. CJNE
4. SETB

Q.9 a) Explain addressing modes of 8051 with suitable examples 08

b) WAP to divide two numbers from external memory locating 5000h and 5001h and store quotient in 5002h and remained in 5003h 07

Q.10 Write short notes (any three) 15

a) Serial communication using 8051
b) Port 3 of 8051
c) TMOD register
d) Keyboard interfacing with 8051

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Total No. of Printed Pages:4

SUBJECT CODE NO:- K-85
FACULTY OF ENGINEERING AND TECHNOLOGY
T.E.(EC/ECT/IEC/E&C) Examination Oct/Nov 2016
Electronics System Design
(Revised)

[Time: Three Hours] **[Max. Marks:80]**

Please check whether you have got the right question paper.

N.B
i) Q.No.1 and Q.No.6 are compulsory.
ii) Solve any two questions from the remaining questions of each section A and B.
iii) Assume suitable components and data wherever necessary.
iv) Figures to the right indicate full marks.
v) Required data sheet is provided.

Section A

Q.1 i) Explain the types and selection criteria for transistors in an electronics circuit design. 10
ii) Draw the circuit diagram of instrumentation amplifier. State its design specifications.
iii) Why fuse and filter capacitor are required in regulated DC power supply? State their selection criteria's.
iv) List the features and absolute maximum rating of temperature sensor IC LM35.

Q.2 a) Design A.M. detector with following specifications: 08
R_i=8KΩ, f_m=7KHz, F_C = 450KHz M_a=0.7
b) Design an IC circuit regulator to generate a 12V output into a load whose current varies from 100MA to 500MA. The input is 115V rms at 60Hz. 07

Q.3 a) Outline the procedure to design adjustable regulator using LM 317. How output current is increased in such regulator? 08
b) Design a circuit for light intensity measurement using photo diode. 07

.4 a) What is the principle of working of strain gauge? How it is used for measurement of strain? 08
b) Design voltage to current amplifier using op amp with following specifications: 07
$I_i = \frac{v_i}{1k\Omega}$, assume grounded load.

Q.5 a) By using 78S40 IC design a step down switching regulator to give the output voltage of 5V at a maximum load current of 600 MA for the input voltage of 10V. The ripple in the output voltage be less than 20mV_{pp}. 08
b) Design schmitt trigger with limitor. Limiting should occur at +6V and -4V with scope of the limiting characteristics as -1/25. 07
Assume V_{REF}=10V, R_A=50KΩ, V_{ON}=0.7V and R_f=100Ω.

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Section B

Q.6 Solve any two 10

i) Explain PCB design rules for digital circuits.
ii) Explain the importance of grounding and shielding.
iii) What is reliability of the product? What are the considerations for reliability?
iv) Explain the features of IC 565.

Q.7 a) Design decade counter circuit using IC 7490. 08

b) Design a $3\frac{1}{2}$ digit DVM for measuring the input voltage from 2V to 10V DC using IC 7106. 07

Q.8 a) Explain finite state machine in detail. 07

b) Design a mono stable multi vibrator using IC 555 with following specifications. 08

V_{CC}=5V
Pause width = 1m sec
Draw the waveforms at pin Nos. 2,7 and 3 with same reference.

Q.9 a) Explain the working of function generator using IC L 8038. 08

b) Explain heat transfer fundamentals in context with electronics circuit design. 07

Q.10 Write short note on 15

i) Mood and mealy FSM
ii) Lm 380 Audio amplifier
iii) Characteristics of TTL

Data Sheet

1. General purpose transistors :

Device	Type	Icmax	VcEo	Vcbo	Ptmax	Life min	f_r
(1) 2N 2996	NPN	100 mA	18 V	18 V	200 MW	200	200 MHz
(2) BFY 51	NPN	1 Amp	30 V	60 V	800 MW		50 MHz
(3) 2N 3702	PNP	200 mA	25 V	40 V	300 MW		100 MHz
(4) BCY 70	PNP	20 mA	40 V	50 V	300 MW		200 MHz

2. Small Signal Transistors :

(1) BC 107	NPN	100 mA	45 V	50 V	300 MW	110
(2) BC 157	PNP	100 mA	45 V	50 V	300 MW	470

3. Switching Transistors :

(1) 2N 2219 A	NPN	800 mA	40 V	75 V	800 MW	75	200 MHz
(2) 2N 2905	PNP	600 mA	40 V	60 V	600 MW	150	

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4. RF Transistors :

(1) 2N 2969 A	NPN	200 mA	15 V	40 V	360 MW	40	500 MHz
(2) BFY 90	NPN	50 mA	15 V		200 MW		1.4 GHz
(3) BC 177	PNP	100 mA	45 V	50 V	300 MW	75	130 MHz
(4) BC 178	PNP	100 mA	25 V	30 V	300 MW	75	130 MHz

5. Driver Transistors :

(1) 2N 3053	NPN	700 mA	40 V	60 V	800 MW	125	100 MHz
(2) 2N 2905	PNP	1 A	40 V		600 MW	100	

6. Power Transistor :

(1) 2N 3055	NPN	15 A	60 V	100 V	115 W	20	1 MHz
(2) BD 131	NPN	3 A	45 V	70 V	15 W	20	60 MHz
(3) BD 132	PNP	3 A	45 V	45 V	15 W	20	60 MHz
(4) TIP 31 A	NPN	3 A	60 V	60 V	40 W	10	8 MHz
(5) TIP 32 A	PNP	3 A	60 V		40 W		8 MHz
(6) SL 100	NPN	0.5 A	50 V		4 W	40	
(7) SK 100	PNP	0.5 A	50 V		4 W	40	

7. Darlington Transistor:

(1) TIP 132	NPN	8 A	100 V	100 V	70 W	1000	1 MHz
(2) TIP 137	PNP	8 A	100 V	100 V	70 W	1000	1 MHz

1. Resistor std. Values (Ω, KΩ, MΩ with fixed values):

1.0, 1.1, 1.2, 1.3, 1.5, 1.6, 1.6, 2.0, 2.2, 2.4, 2.7, 3.0, 3.3, 3.6, 3.9, 4.3, 4.7, 5.1, 5.6, 6.2, 6.8, 7.5, 8.2, 9.1

2. Capacitance Values (µF, nF,pF):

0.1, 0.15, 0.22, 0.33, 0.47, 0.60 and multiples of 10

3. Inductance values (H,mH,µH):

1.0, 1.1, 1.2, 1.3, 1.5, 1.6, 1.8, 2.0, 2.2, 2.4, 2.7, 3.0, 3.3, 3.6, 3.9, 3.9, 4.7, 5.1, 5.6, 6.2, 6.8, 7.5, 3.2, 9.1

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4. Diodes :

Normal :	**Device**	**PIV**	**I_f**
	EC 103	100 V	3 Amp
	EC 403	400 V	3 Amp
Rectifier :	IN 4001	50 V	1 Amp
	IN 4007	1000 V	1 Amp

5. Zener diodes :	**Types No.**	**V_8**	**I_n(mA)**	**Z_n(Ω)**	**I_m(mA)**
	IN 4370	2.4 V	20	30	150
	IN 4371	2.7 V	20	30	135
	IN 4372	3.0 V	20	29	120
	IN 746	3.3 V	20	20	110
	IN 747	3.6 V	20	24	100
	IN 748	3.9 V	20	23	95
	IN 749	4.3 V	20	22	85
	IN 750	4.7 V	20	19	75

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Total No. of Printed Pages:3

SUBJECT CODE NO:- K-152
FACULTY OF ENGINEERING AND TECHNOLOGY
T.E.(EC/ETC/IE/E&C) Examination Oct/Nov 2016
Feedback Control System
(Revised)

[Time: Three Hours] **[Max. Marks:80]**

Please check whether you have got the right question paper.

N.B i) Q.No.1 & 6 are compulsory.
ii) Solve any two questions in each section from Q 2 to 5 & Q.7 to 10.
iii) Figure to the right indicator full marks.
iv) Semi log, graph paper are allowed.
v) Make necessary assumptions & state then clearly.

Section A

Q.1 Solve any two 10

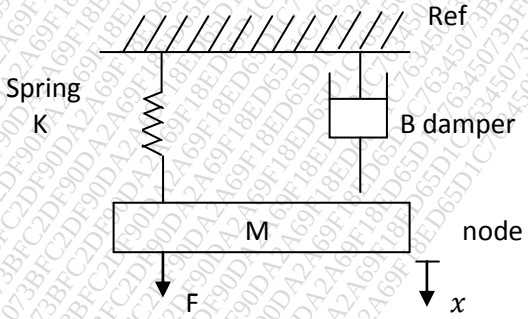
a) Define transfer function. What are its properties? Explain procedure for obtaining T.F.

b) Explain hydraulic system.

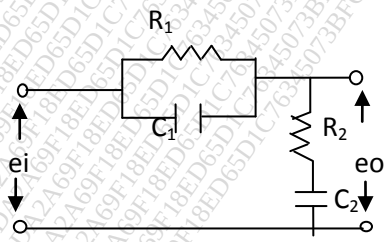
c) The control system having unity feedback has $G(s) = \frac{20}{s(1+4s)(1+s)}$ determine

i) Different static error coe
ii) Steady state error if input $r(t)=2+4t+t^2/2$.

Q.2 a) Draw the force current analogy for figure shown below and draw direct analogous circuit 08



b) Find the T.F. of circuit given in figure 07



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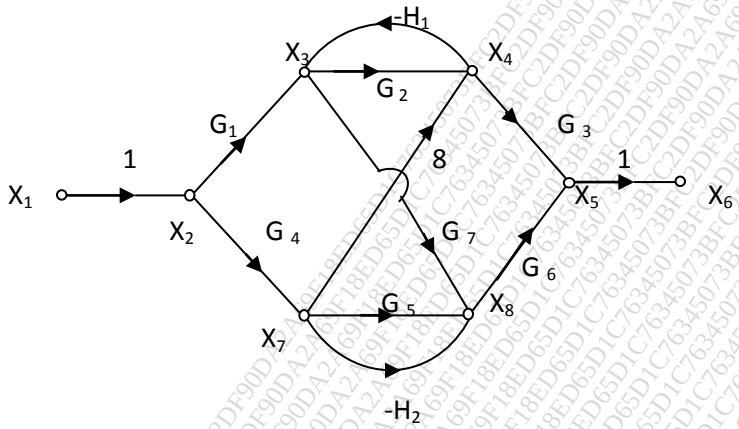
Q.3 a) State & explain block diagram reduction rules. 07

b) For the following SFG obtain the ratio of C(s)/R(s)=X_6/X_1 using Mason's gain formula. 08



Q.4 a) What are the design specifications of second order system explain the derivation of unit step response of second order system 08

b) Find the time domain specifications for $\frac{C(s)}{R(s)} = \frac{1}{s^2+s+1}$ 07

Q.5 Write short note on (any three) 15

1) Properties of Z-transform
2) Mason's gain formula
3) Synchro transmitter & receiver
4) Potentiometer as a error detector
5) Concept of transfer function.

Section B

Q.6 Write any two questions 10

1) Concept of stability
2) Frequency domain specifications
3) Steps of root locus technique

Q.7 a) Sketch the root locus of a unity feedback control system with an open 100 P T.F. 08

$$G(s) = \frac{k}{S(s+2)(s+4)}$$

b) Check the following system is stable or unstable using R-H criteria 07
$S^6+3s^5+9s^3+8s^2+6s+4=0$

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Q.8 a) Construct the bode plot. from bode plot find GM & PM comment on stability for T.F. unity feedback 15

$$G(s) = \frac{10}{s(s+1)(s+5)}$$

Q.9 a) Check for observability 08

$$X = \begin{bmatrix} 0 & 1 \\ 2 & -3 \end{bmatrix} \begin{matrix} x_1 \\ x_2 \end{matrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} V$$

$$Y = [1 \quad 1]$$

b) Explain Nyquist stability criteria in detail. 07

Q.10 Write short notes on (any three) 15

1) Temperature sensor
2) Gain margin & phase margin
3) Polar plots
4) Relays
5) Programmable logic controllers

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Total No. of Printed Pages:2

SUBJECT CODE NO:- K-174
FACULTY OF ENGINEERING AND TECHNOLOGY
T.E.(EC/ECT/IEC/E&C) Examination Oct/Nov 2016
Electromagnetic Engineering
(Revised)

[Time:Three Hours] **[Max. Marks:80]**

Please check whether you have got the right question paper.

N.B
i) Q 1 and Q 6 are compulsory.
ii) Solve any two questions from Q.2, Q.3, Q,4 and Q,5 in section A.
iii) Solve any two questions from Q.7, Q.8, Q.9 and Q 10 in section B.
iv) Figures to the right indicate full marks.
v) Assume suitable data wherever necessary and mention it clearly.

Section A

Q.1 Solve any 2 10
a) Explain Gauss Law
b) Derive divergence theorem ($\oint D.ds = \int \nabla.D.dv$)
c) Derive boundary conditions for perfect dielectric materials.
d) Write the table of dot products of unit vectors in cylindrical and rectangular coordinate systems.

Q.2 a) Express in cylindrical components 07
i) The vector from C (3,2,-7) to D (-1,-4,2)
ii) A unit vector at D directed towards C
iii) A unit vector at D directed towards origin.
b) Transform the vector field H= (A/ρ) a_ρ Where A is constant, from cylindrical coordinates to spherical coordinates. 08

Q.3 a) A uniform volume charge density of $0.2\ \mu C/m^2$ is present throughout the spherical shell extending from r=3 cm to r=5cm. If ρ_v=0 elsewhere find 07
i) The total charge present in the shell and
ii) r_1 if half the total charge is located in the region 3cm<r<r_1
b) If $\bar{E} = -8 \times y a_x - 4x^2 a_y + a_z\ V/m$ find the work done in carrying a 6 C charge from M(1,8,5) to N (2,18,6) along the path: $y=3x^2+z$, z=x+4 08

Q.4 a) Two uniform line charge 8 nC/m each are located at x=1, z=2 and at x=--1, y=2 in free space. If the potential at the origin is 100 V find V at P (4,1,3). 07
b) In cylindrical coordinates $J = 10e^{-100r} a_\phi\ A/m^2$. Find the current crossing the region 08
$0.01 \le r \le 0.02$m, $0 < z \le 1$m and intersection of this region with the ϕ = constant plane.

Q.5 a) Give the potential V = 100 ($x^2 - y^2$) and a point P (2,--1, 3) that is stipulated to lie on a conductor free space boundary. Find V, $\bar{E}$,$\bar{D}$ and ρ_s at point P. 10
b) Derive the expression of potential field due to system of charges. 05

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Section B

Q.6 Solve any 2 10

i) Derive the equation of average power density in a uniform plane wave propagating in perfect dielectric.

ii) Explain skin depth.

iii) Derive boundary conditions for static magnetic field.

iv) Derive the equation of total power in a uniform plane wave by Poynting theorem.

Q.7 a) i) Find $\bar{H}$ in rectangular components at P(2,3,4) if there is a current filament on the z axis carrying 8 mA in the a_z direction. ii) Repeat if the filament is located at x=-1, y=2. 07

b) Find $\bar{H}$ at P (2,3,5) in Cartesian coordinates if there is an infinitely long current filament passing through the origin and point C. The current of 50A is directed from the origin to C where the location of C is C (0,0,1). 08

Q.8 a) In a material for which σ=5 S /m , $\in_r$=1, the electric field intensity is E=250* sin(10^{10}t)V/m. find the conduction current density and displacement current density for the given field. 07

b) Find the amplitude of the displacement current density 08

i) In the air near a car antenna

ii) In an air space within a large transformer where

$\bar{H}$ =106 cos (377t+1.2566*10-6*z)a_y A/m

Q.9 a) A lossy dielectric is characterized by $\in_r$=2.5, μ_r=4 and $\sigma=10^{-3}$ S/m at frequency 10 MHz. Find 07
i) attenuation constant ii) intrinsic impedance

b) for a 30 GHz uniform plane wave calculate the wavelength and attenuation if the wave is propagating 08
in a non-magnetic material for which i) $\in_r$=1 and σ=0 ii) $\in_r$ = 1.01 and $\sigma=10^{-3}$ S/m
iii) $\in_r$=2.1 and σ = 5 S/m

Q.10 a) Let $\bar{H} = -y(x^2 + y^2)a_x + x(x^2 + y^2)a_y$ A/m in the z=0 plane for -- 5 ≤ x ≤ 5m and -- 5 ≤ y ≤ 5 m 10
Find the total current passing through the z=0 plane in the a_z direction inside the rectangle --1<x<1m and –2<y<2 m by ∇XH=J

b) Explain faraday's law in detail 05

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Total No. of Printed Pages:2

SUBJECT CODE NO:- K-199
FACULTY OF ENGINEERING AND TECHNOLOGY
T.E.(EC/ECT/IEC/E&C) Examination Oct/Nov 2016
Microprocessors & Peripheral
(Revised)

[Time:Three Hours] **[Max. Marks:80]**

Please check whether you have got the right question paper.

N.B i) Q.1 and Q.6 are compulsory.
ii) Solve any two questions from remaining in each section.
iii) Assume suitable additional data, if necessary.

Section A

Q.1 Solve any two- 10
a) List and explain various programming tool involved with 8085 programming.
b) What is bus? Explain the bus organisation of 8085 and the role of bus in 8085.
c) What is stack pointer? Explain PUSH and POP instructions in detail.
d) Compare and contrast memory mapped I/O with I/O mapped I/O.

Q.2 a) Draw the timing diagram of the instruction LHLD 200H. 08
b) Write an ALP to add only positive numbers in a block of 100 bytes from location 7000H. 07

Q.3 a) What is interrupt? Describe 8085 interrupt structure in detail. 08
b) Draw and explain the timing diagram of ADD 05H. 07

Q.4 a) Write a program to generate a time delay of 100 msec. 08
b) Explain how call instruction is executed in 8085 microprocessor. 07

Q.5 a) Design memory system for 8085 such that it should contain 8K byte of ERROM and 8K byte of RAM. .give memory map for EPROM and RAM. 08
b) What you mean by data transfer schemes. What are the different data transfer scheme available .Explain programmed data transfer schemes. 07

Section B

Q.6 Attempt any two of the following 10
i) BSR mode of 8255.
ii) Mode 3 of 8253.
iii) Salient features with block diagram of 8259.
iv) Speed control of DC motor.

Q.7 a) Design two digit decimal counters which will count from 00 to 99 continuously using seven segment display. Give 8085 based program for this. 08
b) With the help of neat diagram explain ADC 0809 interfacing with 8085. 07

Q.8 a) An 8253 is connected to 1 MHZ clock. It is to be used to generate square wave signal of 1KHz.freqvency. Give interfacing ckt and program. 08
b) Explain mode 1 and mode 3 of 8253 with timing diagram. 07

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Q.9	a)	Explain how you will use 8155 time.	08
	b)	Explain initialization sequence of 8259 with ICW's explanation.	07
Q.10	a)	What is a logic analysis? With the help of diagram explain it.	08
	b)	Explain measurement of voltage by using 8085 microprocessor.	07

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Total No. of Printed Pages:1

SUBJECT CODE NO:- K-299
FACULTY OF ENGINEERING AND TECHNOLOGY
T.E.(EC/ECT/IEC/E&C) Examination Oct/Nov 2016
Digital Signal Processing
(Revised)

[Time: Three Hours] **[Max. Marks:80]**

Please check whether you have got the right question paper.

N.B i) Q.No.1 and Q.No.6 are compulsory.
ii) Solve any two questions from Q. 2 to 5 & Q. 7 to 10.
iii) Assume suitable data is necessary.

Q.1 Solve any two from following 10
a) Draw butterfly structure of DIT radix-2 FFT algorithm for 8-pt DFT.
b) What is z- transform? Obtain 2T of standard test signal.
c) What are the applications of DSP? Explain.
d) Explain relation between LT & ZT.

Q.2 a) Explain properties of z-transform. 07
b) Obtain IZT of following $x(z) = \frac{z}{3z^2-4z+1} \quad for \quad |z| > \left|\frac{1}{3}\right|$ by using partial fraction expansion method. 08

Q.3 a) Explain with example overlap add method of long data sequence. 07
b) Obtain 8Pt DFT of x(n)= {1,1,1,1}. 08

Q.4 a) State & explain properties of DFT. 07
b) Obtain circular convolution by concentric circle method of $x_1(n) = \{1, -1, -2, 3, -1\}$ 08
$x_2(n) = \{1,1,1\}$.

Q.5 a) Obtain IDFT of following sequence x(k)={6,-2+2j, -2,-2,-2j}. 07
b) Obtain ZT of following $x(n) = \cos\left[\frac{n\pi}{4} + \propto\right].u(n)$. 08

Q.6 Solve any two from following. 10
a) Give the requirements to design ideal filter.
b) Explain frequency transformation in digital filter.
c) Explain difference between IIR & FIR filter.
d) Write note on product quantization error.

Q.7 a) Design system function of digital filter using approximation of derivative method for $H(s) = \frac{1}{(s+0.1)^2+g}$ 08
b) Explain bilinear transformation to design IIR filter. 07

Q.8 a) Explain various windows used to design FIR filter. 07
b) Design HP FIR filter of length using hanning window with cut off frequency 1 rad /sec. 08

Q.9 a) Design a second order discrete time Butterworth filter with cut off frequency 1 KHz & sampling frequency of 10^4 samples/sec. Using bilinear transformation method. 10
b) Write note on rectangular window in detail. 05

Q.10 a) Explain quantization by truncation & rounding. 07
b) What is FIR filter? Explain Gibb's phenomenon. 08

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-Total No. of Printed Pages:2

SUBJECT CODE NO:- K-361
FACULTY OF ENGINEERING AND TECHNOLOGY
T.E.(I E) Examination Oct/Nov 2016
Industrial Drives & Control
(Revised)

[Time: Three Hours] **[Max. Marks:80]**

Please check whether you have got the right question paper.

N.B
i) Q.No.1 from section A and Q.No.6 from section B is compulsory.
ii) Attempt any two questions from remaining questions of section A and B each.
iii) Assume suitable data, if necessary.
iv) Figures to the right indicate full marks.

Section A

Q.1 Solve any two. 10

i) What do you mean by electric drive? Mention factors which decide the choice of electric drive.
ii) Explain clearly the driving motors used in cement industry for different operations.
iii) Draw the block diagram of voltage source inverter fed squirrel cage induction motor and explain briefly its operation.
iv) Explain the load equalization for fluctuating loads in drives.

Q.2 a) Explain single phase half-controlled rectifier of dc separately excited motor with continuous and discontinues conduction. 08

b) A 220V, 50A 1500rpm separately excited dc motor has an armature resistance of 0.5Ω fed from three phase fully controlled converter. AC source has a line voltage of 440V, 50Hz. A star –delta connected transformer is used to feed the armature so that the motor terminal voltage equal to rated voltage when converter firing angle is zero. 07

i) Calculate transformer turns ratio
ii) Determine α when : a) Motor is running at 1200rpm and rated torque
b) Motor is running at 800rpm and twice the rated torque. Assume Continuous conduction.

Q.3 a) Draw the block diagram of slip recovery system for wound rotor Induction motor and explain its operation. 08

b) A star-connected 3-phase, 50 Hz, 6 pole, slip ring induction motor has following data: 07
Rating: 400V, 50Hz, 960 rpm and R_1=0.08Ω, R_2=0.1Ω, X_1=X_2=0.3Ω, J=10kg-m^2. Motor is to be stopped from its no load under reverse voltage braking operation.

i) Find the value of external resistance to be inserted in rotor circuit so that braking process will take minimum time and
ii) Find energy loss in motor

Q.4 a) Explain dynamic braking of separately excited dc motor by chopper control. 08

b) Justify variable frequency control of induction motor is more efficient than stator voltage control. 07

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Q.5 Write a short note on: 15

i) Drives used in Rolling mill
ii) Static rotor resistance control of an induction motor
iii) Dynamic braking of 3 phase induction motor

Section B

Q.6 Attempt any two. 10

i) What are the applications of stepper motor?
ii) State and elaborate desired characteristics of traction motors.
iii) How load torques in a drive system is classified? Explain its various components.
iv) State advantages of electric traction.

Q.7 a) Draw the block diagram of cycloconverter fed synchronous motor and explain its operation. 07

b) What are different types of synchronous motors? Explain the operation of permanent magnet synchronous motor. 08

Q.8 a) What are the different types of electric traction services? Explain the traction drive for main line trains. 07

b) What is tractive effort? Obtain complete expression for total tractive effort using usual notations. 08

Q.9 a) A drive has following equations for motor and load torque: $T = (1 + 2w_m)$ and $T_1 = 3w_m$. Obtain the equilibrium points and determine their steady state stability. 07

b) Explain various motor duty types with one example each. 08

Q.10 Write short note on: 15

i) Dynamics of electrical drives
ii) Advantages of using motors compared to engine drive
iii) Mechanism of train movement

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Total No. of Printed Pages:2

SUBJECT CODE NO:- K-232
FACULTY OF ENGINEERING AND TECHNOLOGY
T.E.(ECT/E&C) Examination Oct/Nov 2016
Digital Communication
(Revised)

[Time: Three Hours] **[Max. Marks:80]**

Please check whether you have got the right question paper.

N.B i) Q.No.1 and Q.6 are compulsory.
ii) Solve any two questions from Q.No2 to Q.No5.
iii) Solve any two questions from Q.No7 to Q.No10.
iv) Assume suitable data if necessary.

Section A

Q.1 Attempt any two questions. 10

a) Find the Nyquist rate and the Nyquist interval for the signal.
$x(t) = \frac{1}{2\pi}\cos(4000\pi t)\cos(1000\pi t)$
b) Define Companding. Draw model of companding with characteristics.
c) Draw and explain generation of PPM with waveform.
d) Describe effect of under sampling with waveform.

Q.2 a) Derive the mathematical expression for pulse Amplitude modulation with aperture effect. 08

b) Draw and explain Block diagram of Digital communication system. 07

Q.3 a) List various sampling techniques. A band limited signal x (t) is sampled by train of rectangular pulses of width 'τ'. Determine spectrum of flat – top sample signals. 08

b) State and explain sampling theorem for low pass signals in time domain. 07

Q.4 a) How to reconstruct the original waveform using PCM receiver? Discuss transmission bandwidth in a PCM system. 08

07

b) A PCM system uses a uniform quantizer followed by a 7-bit binary encoder. The bit rate of the system is 50×10^6 bits/ sec.
i) What is the maximum message signal Bandwidth?
ii) Calculate the output signal to quantization noise ratio.

Q.5 Write short note on 15
i) A law and μ law companding
ii) Performance & comparison of various sampling techniques.
iii) Quantization process.

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Section – B

Q.6 Solve any two questions. 10

i) Define Inter symbol interference. How ISI can be removed from the system?

ii) Illustrate the signal space representation of BFSK & Bandwidth.

iii) Describe slow & fast frequency hopping in FHSS.

iv) Describe effect of Gaussian Noise on Bipolar signals with waveform.

Q.7 a) Draw and explain transmitter & receiver of Adaptive delta modulation. 08

b) Calculate the impulse response for the matched filter. 07

Q.8 a) For the input binary sequence $b(k) = \{1, -1, 1, -1, -1, -1, 1, 1, 1\}$ find the transmitted phase sequence and sketch the transmitted waveform for QPSK. 08

b) Compare BASK, BFSK & BPSK in detail. 07

Q.9 a) With the help of neat block diagram explain how DS-SS signals are generated and detected. 08

b) Define following performance parameters of DSSS : 07

i) Processing gain

ii) Probability error

iii) Jamming margin and what are the application of DSSS?

Q.10 Write short note on 15

a) Drawback of delta modulation

b) Discuss MSK system

c) PN sequence related with spread spectrum.

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Total No. of Printed Pages:2

SUBJECT CODE NO:- K-264
FACULTY OF ENGINEERING AND TECHNOLOGY
T.E.(EC/ECT/IEC/E&C) Examination Oct/Nov 2016
Analog Integrated Circuit & Applications
(Revised)

[Time: Three Hours] **[Max. Marks:80]**

Please check whether you have got the right question paper.

N.B
1. Q.No.1 from section A and Q.No.6 from section B are compulsory.
2. Solve any two questions from Q.2, Q.3, Q.4 and Q.5.
3. Solve any two questions from Q.7, Q.8, Q .9& Q.10.

Section A

Q.1 Write short notes on any two. 10
1) Block dia. of op-Amp.
2) Square wave generator using op-Amp.
3) Mono stable multi vibrator using IC555.
4) Op-Amp Integrator.

Q.2 a) Explain operation of logarithmic amplifier. And derive equation for its output. 08
b) Draw an Instrumentation amplifier using three op-Amp and explain its operation. 07

Q.3 a) Draw the Block dia. of IC555 and explain operation. 07
b) Draw & design wien bridge oscillator using op-Amp for $f_o = 965Hz$ 08

Q.4 a) List the characteristics of an Ideal op-Amp. Draw equivalent ckt and transfer characteristics of an op-amp & explain. 08
b) What is slew rate? List causes of the slew rate & explain its effect on op-Amp ckts. 07

Q.5 a) Explain operation of precision full wave rectifier with ckt. diagram & waveforms. 08
b) Explain operation of Schmitt trigger with ckt. Diagram & waveforms. 07

Section – B

Q.6 Attempt any two. 10
1) Compare active and passive filter design.
2) Explain basic principle of PLL and its transient response.
3) Explain operation of IInd order high pass Butterworth filter.
4) Draw & explain internal B.D of IC723.

Q.7 a) Design IInd order low pass Butterworth filter at a high cut off frequency of 1kHz. 08
b) What is band pass filter? Explain wide band pass filter with ckt. dia. 07

Q.8 a) Draw internal B.D. of PLL IC565 and explain, state its applications. 08
b) A PLL has VCO with k_0=25 KH_O/V and f_c=50 KHz. The amplifier gain is A=2 and phase detector has maximum o/p voltage swing IO.7V. Find the lock range of PLL. Assume filter gain equal to unity. 07

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Q.9 a) Explain step-up regular ckt using switching regulator IC 78S40. 08

b) Design an adjustable voltage regulator using LM317 to specify the following specification. 07
O/p voltage $v_o = 6\ to\ 12v$
O/p current I_o = 1.0 Amp.

Q.10 a) Explain application of PLL as a FSK demodulator with dia. 08

b) What is multiple feedback filters? Explain with diagram. 07

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